intel®

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

OLD

3608, 3628
8K (1K X 8) BIPOLAR PROM

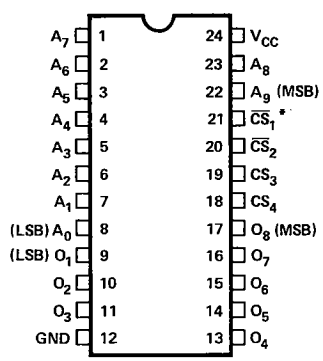
3608, 3628	80 ns Max.
3608-4, 3628-4	100 ns Max.

- **Fast Access Time: 65 ns Typically**
- **Low Power Dissipation: 0.09mW/Bit Typically**
- **Four Chip Select Inputs for Easy Memory Expansion**
- **Open Collector (3608) and Three-State (3628) Outputs**
- **Hermetic 24-Pin DIP**
- **Polycrystalline Silicon Fuses for Higher Fuse Reliability**

The Intel® 3608/3628 are fully decoded 8192 bit PROMs organized as 1024 words by 8 bits. The worst case access time of 80 ns is specified over the 0°C to 75°C temperature range and 5 percent V_{CC} power supply tolerances. There are four chip selects provided to facilitate expanding 3608/3628s into larger PROM arrays. The PROMs are a Schottky clamped TTL memory array with polycrystalline silicon fuses. All outputs are initially high and logic low levels can be electrically programmed in selected bit locations.

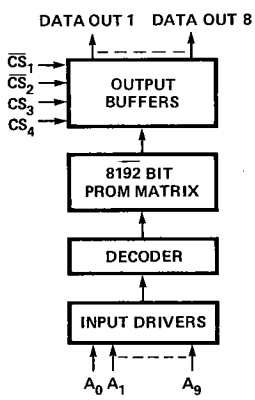
Prior to the 8192 bit 3608/3628, the highest density bipolar PROM available was 4096 bits. The high density of the 3608/3628 now easily doubles the capacity without an increase in area on existing designs currently using 512 words by 8 bit PROMs. There is also little, if any, penalty in power since the 3608/3628 power/bit is approximately one-half that of 4K PROMs. The 3608/3628 are packaged in a hermetic 24-pin dual in-line package.

PIN CONFIGURATION

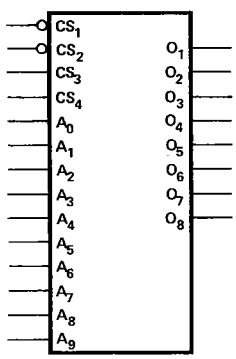


*PROGRAMMING PIN

BLOCK DIAGRAM



LOGIC SYMBOL



PIN NAMES

$A_0 - A_9$	ADDRESS INPUTS
$\overline{CS}_1 - \overline{CS}_2$, $CS_3 - CS_4$	CHIP SELECT INPUTS[1]
$O_1 - O_8$	DATA OUTPUTS

[1] To select the PROM $\overline{CS}_1 = \overline{CS}_2 = V_{IL}$ and $CS_3 = CS_4 = V_{IH}$

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1V to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS: All Limits Apply for V_{CC}= +5.0V ±5%, T_A= 0°C to +75°C

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.[1]	Max.	Unit	
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC}=5.25V, V_A=0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC}=5.25V, V_S=0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC}=5.25V, V_A=5.25V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC}=5.25V, V_S=5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.75V, I_A=-10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC}=4.75V, I_S=-10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC}=4.75V, I_{OL}=15mA
I_{CEX}	3608 and 3608-4 Output Leakage Current			100	μA	V_{CC}=5.25V, V_{CE}=5.25V
I_{CC}	Power Supply Current		150	190	mA	V_{CC} =5.25V, V_{A0}→V_{A9}=0V, PROM deselected
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC}=5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC}=5.0V

3628,3628-4 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance State			100	μA	V_O=5.25V or 0.45V, V_{CC}=5.25V, $\overline{CS}_1$=$\overline{CS}_2$=2.4V
I_{SC}[2]	Output Short Circuit Current	-15	-25	-60	mA	V_{CC}=5.00V, T_A=25°C, V_O = 0V
V_{OH}	Output High Voltage	2.4	3.4		V	I_{OH}=-2.4mA, V_{CC} = 4.75V

NOTES: 1. Typical values are at 25°C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A.C. CHARACTERISTICS V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	MAX. LIMITS 3608 3628	MAX. LIMITS 3608-4 3628-4	UNIT	CONDITIONS
t_A	Address to Output Delay	80	100	ns	$\overline{CS}_1 = \overline{CS}_2 = V_{IL}$ and $CS_3 = CS_4 = V_{IH}$ to select the PROM.
t_{EN}	Output Enable Time	40	45	ns	
t_{DIS}	Output Disable Time	40	45	ns	

CAPACITANCE[1] T_A = 25°C, f = 1 MHz

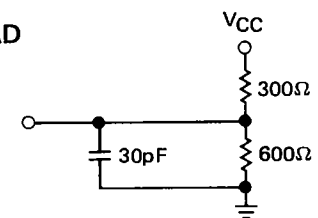
SYMBOL	PARAMETER	TYP. LIMITS	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS

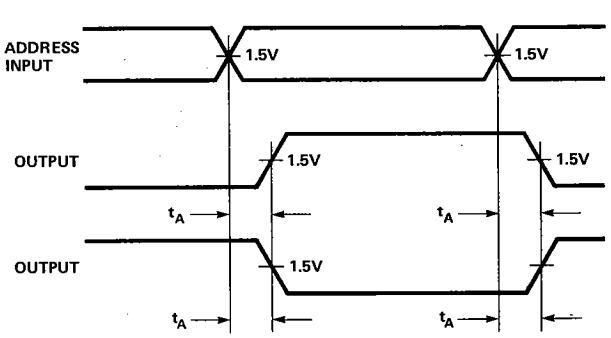
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15mA TEST LOAD

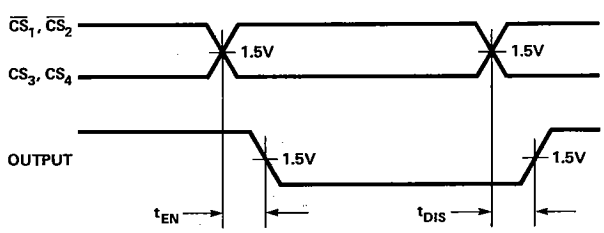


WAVEFORMS

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY



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